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Computer Architecture – Assignment 4

Monroe College

Assignment 4

Exercise 1:

**Assembly Language Program**

1: MOV R3, R7

2: LD R8, (R3)

3: ADD R3, R3, 4

4: LOAD R9, (R3)

5: BNE R8, R9, L3

(A)

**RAW Dependency:**

1: MOV R3, R7

2: LD R8, (R3)

**WAR Dependency:**

3: ADD R3, R3, 4

4: LOAD R9, (R3)

**WAW Dependency:**

4: LOAD R9, (R3)

5: BNE R8, R9, L3

(B)

Data dependency is a situation in which a program instruction refers to the data of preceding instruction. So in this condition without executing previous instructions, current instruct will not get the data or the true data value is dependent on previous instructions.

Data Hazard is the situation which prevent the next instruction in the instruction stream from executing in its designated clock cycle. Data hazards creates because the instruction has data dependency from previous instruction cycle, and without receiving data from that it cannot be execute in designated execution cycle.

EXERCISE 2:

(A)

Bypass is done to avoid hazard or bubble in the pipeline cycle by bypassing the value to other instruction as soon as available. Bypassing is not possible to use each and every time because some instruction may require to finish complete cycle and then only it can pass data to other cycle.

(B)

**Execution without bypassing**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Instruction  Number | Clock Number | | | | | | | | | | | | | |
| load | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |
| Instruction i | IF | ID | EX | MEM | WR |  |  |  |  |  |  |  |  |  |
| i + 1 |  | IF | ID | Stall | Stall | EX | MEM | WR |  |  |  |  |  |  |
| i + 2 |  |  | IF | ID | Stall | Stall | Stall | Stall | EX | MEM | WR |  |  |  |
| i + 3 |  |  |  | IF | ID | Stall | Stall | Stall | Stall | Stall | Stall | EX | MEM | WR |

Execution without bypass takes 14 clock numbers to finish 3 instruction cycle

**Execution with Bypass shown as mentioned figure**

Instruction of bypass mentioned as below

* bypass from the output of the MEM stage to the EX stage

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Instruction  Number | Clock Number | | | | | | | | | | |
| load | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
| Instruction i | IF | ID | EX | MEM | WR |  |  |  |  |  |  |
| i + 1 |  | IF | ID | Stall | EX | MEM | WR |  |  |  |  |
| i + 2 |  |  | IF | ID | Stall | Stall | EX | MEM | WR |  |  |
| i + 3 |  |  |  | IF | ID | Stall | Stall | Stall | EX | MEM | WR |

With Bypass 3 instruction cycle will finish in 11 clock numbers

So, with Bypass (11 clock numbers) execution time reduced then without bypass (14 Clock numbers).

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